CLAIMS:

1. A method, comprising:

receiving a plurality of packets with audio information sent using a first timing signal; and

reproducing said audio information using a second timing signal and compensating for time differences between said first and second timing signals using a circular buffer with a variable read out location.

2. The method of claim 1, wherein said circular buffer comprises a plurality of buffer locations.

3. The method of claim 2, further comprising building a histogram to represent a probability distribution for a given set of network delays, said histogram having a plurality of levels with each level representing a frequency of network delay, and with each level corresponding to a buffer location for said circular buffer.

4. The method of claim 3, wherein said reproducing comprises:

determining a first delay value for each packet;

storing each packet in a buffer location using said first delay value;

updating said histogram using said first delay value;

determining a read out location for said circular buffer; and

reading each packet from said buffer using said read out location.

5. The method of claim 4, wherein said storing comprises:

determining a second delay value for each packet; and

storing each packet in a buffer location corresponding to said second delay value.

6. The method of claim 5, wherein said determining said second delay value comprises:

retrieving a third delay value;

comparing said first delay value with said third delay value; and

determining said second delay value in accordance with said comparison.

7. The method of claim 6, wherein said first delay value represents a network delay, said second delay value represents a packet delay value, and said third delay value represents an optimal delay value.

8. The method of claim 4, wherein said updating said histogram comprises:

estimating a time difference between said first and second timing signals;

comparing said time difference to a threshold parameter; and

updating said histogram in accordance with said comparison.

9. The method of claim 8, wherein said estimating said time difference comprises:

determining an average packet delay value for said plurality of packets using said histogram on a periodic basis;

analyzing said average delays for a linear change; and

estimating said time difference based on said linear change.

10. The method of claim 9, wherein said time difference is greater than said threshold parameter, and updating said histogram in accordance with said comparison comprises assigning each level a new buffer location within said circular buffer.

11. The method of claim 10, wherein said circular buffer includes a jitter buffer comprising a subset of said buffer locations, with said jitter buffer having a start buffer location and an end buffer location, and said histogram has a start level and an end level, and said assigning comprises:

assigning said end level corresponding to said end buffer location to a next buffer location of said circular buffer; and

shifting said remaining levels by one buffer location towards said end buffer location.

12 The method of claim 11, wherein determining said read out location comprises determining a buffer location corresponding to said end level.

13. A system, comprising:

a first wireless transceiver;

an omnidirectional antenna to couple to said first wireless transceiver; and

a jitter buffer module (JBM) connected to said first wireless transceiver, said JBM further comprising a Clock Compensation Module (CCM).

14. The system of claim 13, wherein said system further comprises:

an encoder connected to said first wireless transceiver; and

a first timing device connected to said encoder and said first wireless transceiver.

15. The system of claim 14, further comprising:

a second wireless transceiver;

an omnidirectional antenna to couple to said second wireless transceiver;

a JBM connected to said second wireless transceiver, said JBM having a CCM; and

wherein said second wireless transceiver further comprises a decoder connected to said second wireless transceiver, and a second timing device connected to said decoder and said second wireless transceiver.

16. The system of claim 15, wherein said JBM further comprises:

a circular buffer; and

a Buffer Management Module (BMM) connected to said circular buffer.

17. The system of claim 16, wherein said CCM estimates a clock differential value between said first and second timing devices using an average packet delay value from a

histogram representing a distributional curve of frequencies of network delays, and sends said clock differential value to said BMM.

18. The system of claim 17, wherein said BMM receives said clock differential value from said CCM, and delays each packet a set amount of time using said clock differential value.

19. The system of claim 18, wherein said circular buffer comprises a plurality of buffer locations to store audio information, with a subset of said buffer locations each corresponding to a level from said histogram.

20. The system of claim 19, wherein said BMM delays each packet by selecting a buffer location to store each packet.

21. The system of claim 20, wherein said BMM modifies which buffer location correspond to which level in accordance with said clock differential value.

22. An apparatus, comprising:

a receiver; and

a Jitter Buffer Module (JBM) connected to said receiver, said JBM further comprising a Clock Compensation Module (CCM).

23. The apparatus of claim 22, wherein said JBM further comprises:

a circular buffer; and

a Buffer Management Module (BMM) connected to said circular buffer.

24. The apparatus of claim 23, wherein said CCM estimates a clock differential value between a first and second timing devices using an average packet delay value from a histogram representing a distributional curve of frequencies of network delays, and sends said clock differential value to said BMM.

25. The apparatus of claim 24, wherein said BMM receives said clock differential value from said CCM, and delays each packet a set amount of time using said clock differential value.

26. The apparatus of claim 25, wherein said circular buffer comprises a plurality of buffer locations to store audio information, with a subset of said buffer locations each corresponding to a level from said histogram.

27. The apparatus of claim 26, wherein said BMM delays each packet by selecting a buffer location to store each packet.

28. The apparatus of claim 27, wherein said BMM modifies which buffer location correspond to which level in accordance with said clock differential value.

29. An article comprising:

a storage medium;

said storage medium including stored instructions that, when executed by a processor, result in receiving a plurality of packets with audio information sent using a first timing signal, and reproducing said audio information using a second timing signal and compensating for time differences between said first and second timing signals using a circular buffer with a variable read out location.

30. The article of claim 29, wherein the stored instructions, when executed by a processor, further result in performing said reproducing by determining a first delay value for each packet, storing each packet in a buffer location using said first delay value, updating said histogram using said first delay value, determining a read out location for said circular buffer, and reading each packet from said buffer using said read out location.